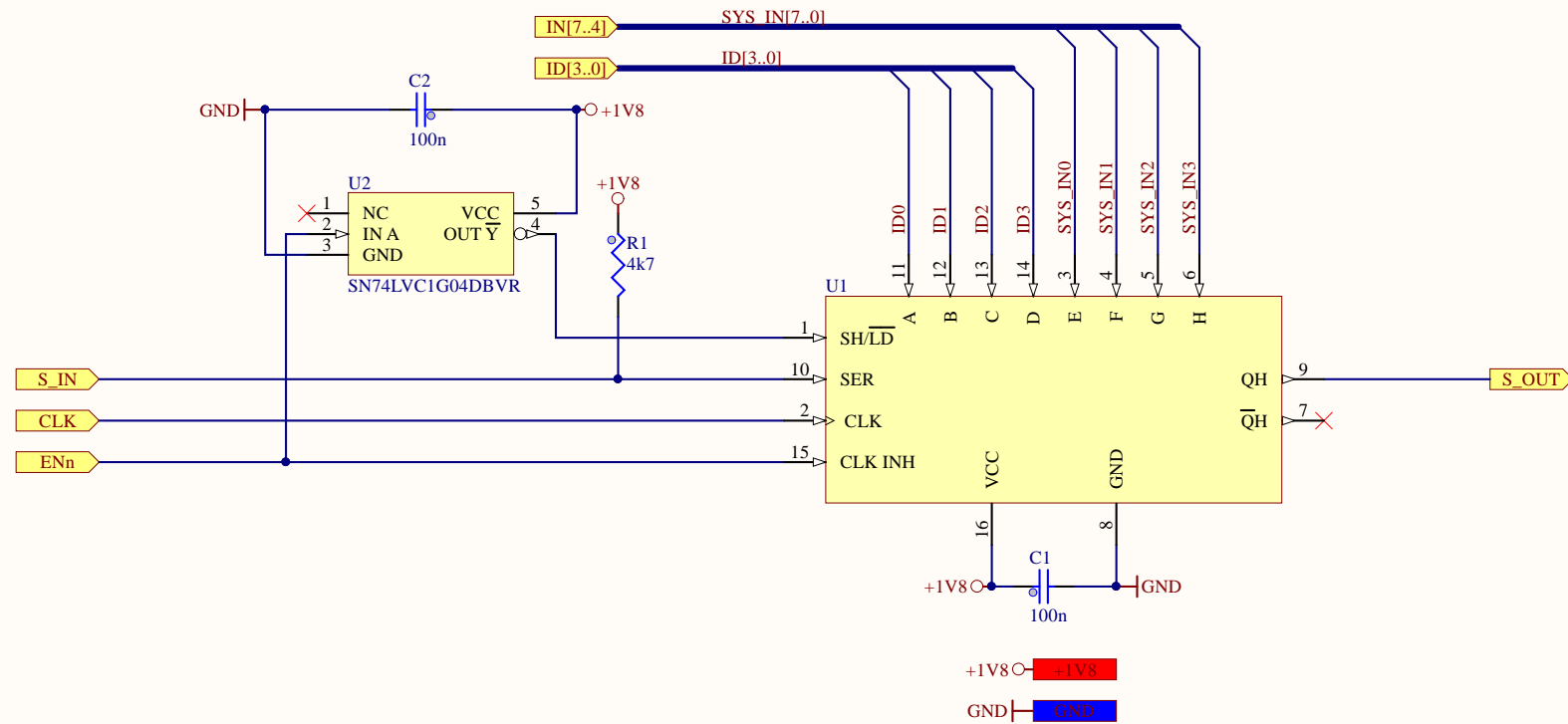


Author: Jiri Kovanda
 Engineer: Jiri Kovanda
 Drawn by: Jiri Kovanda
 Checked by: **
 Approved by: **
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Title: **Turris Mox Peridot - Top**
 Document Number: CZ34NIC010000-1
 Sheet 1 of 15
 Name: CZ34NIC_Card.schdoc

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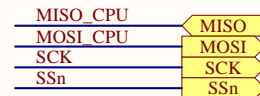
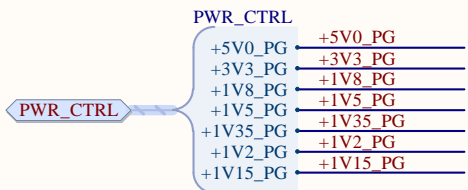
Author: Jiri Kovanda
 Engineer: Jiri Kovanda
 Drawn by: Jiri Kovanda
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Title: **Turris Mox Peridot - ID&In**
 Document Number: CZ34NIC010000-2
 Sheet 2 of 15
 Name: CZ34NIC_SYS_ID&IN.schdoc

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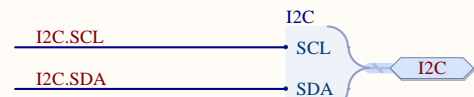
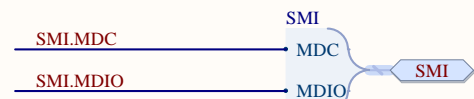
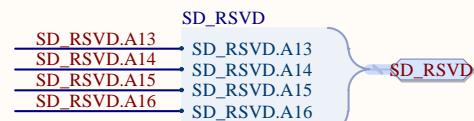
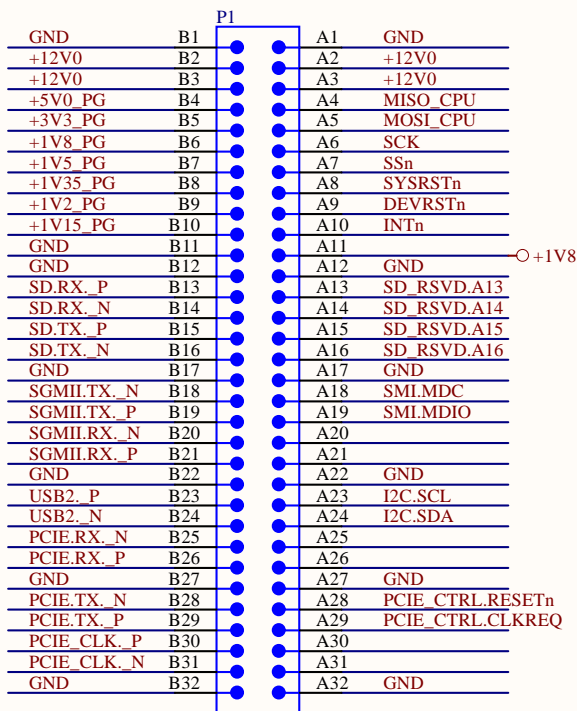
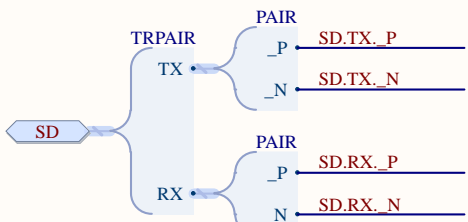

A

A



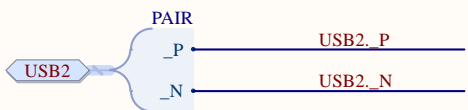
B

B



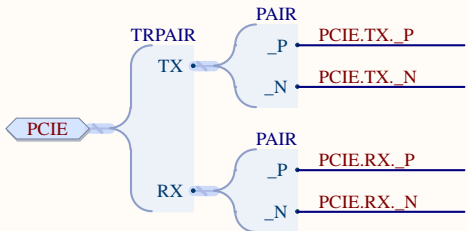
C

C



D

D

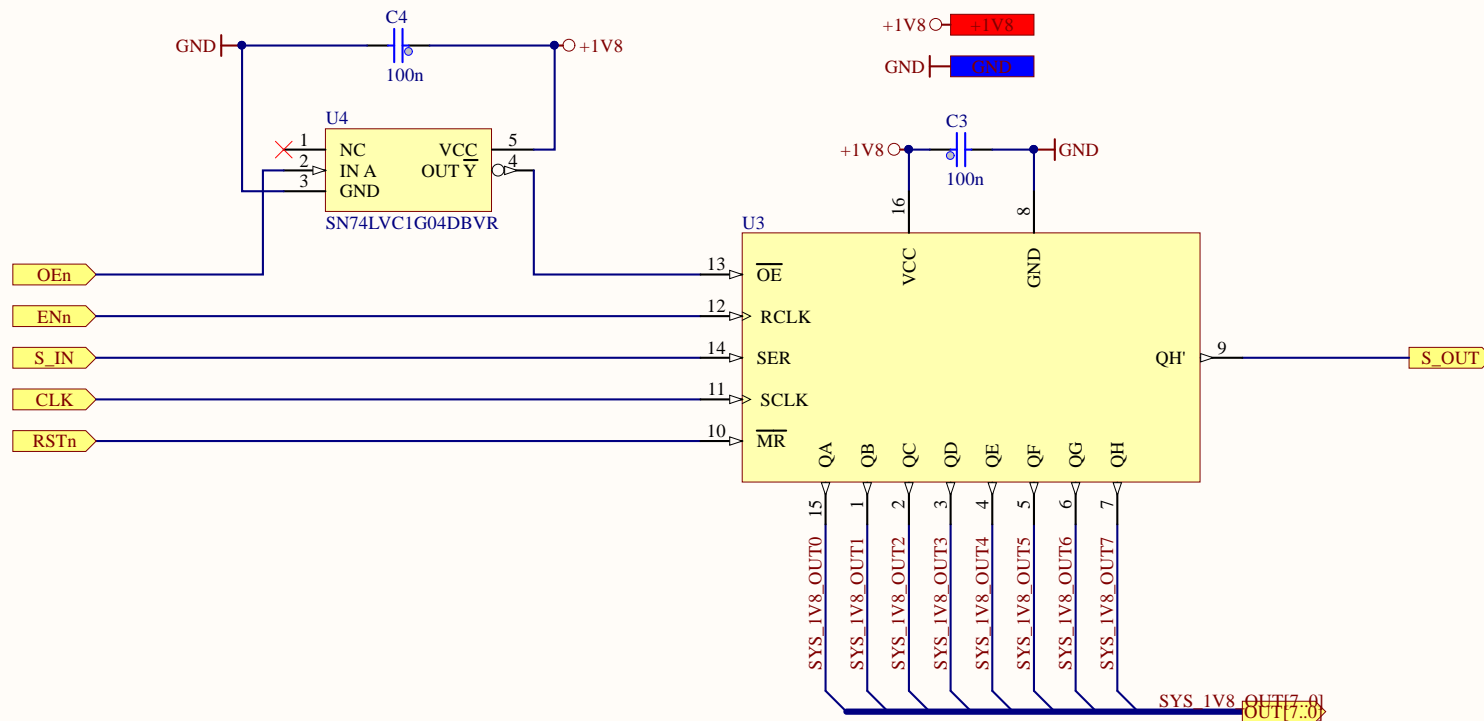


Author: Jiri Kovanda
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 Drawn by: Jiri Kovanda
 Checked by: **
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Title: **Turris Mox Peridot - In CN**

Document Number: CZ34NIC010000-3 Revision: 010000
 Sheet 3 of 15 Date: * *
 Name: CZ34NIC_SYS_IN_CN.SchDoc

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 Engineer: Jiri Kovanda
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Title: **Turris Mox Peridot - Out**
 Document Number: CZ34NIC010000-4
 Sheet 4 of 15
 Name: CZ34NIC_SYS_OUT.schdoc

Revision: 010000
 Date: * *

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A

A

B

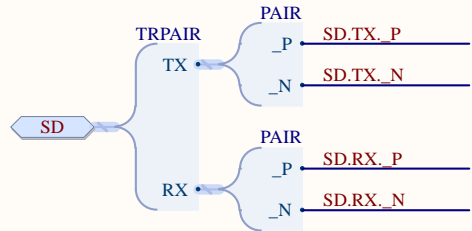
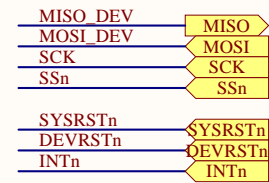
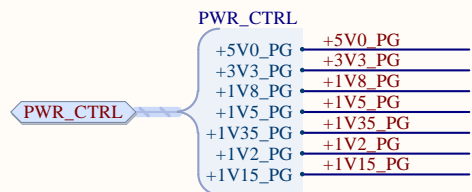
B

C

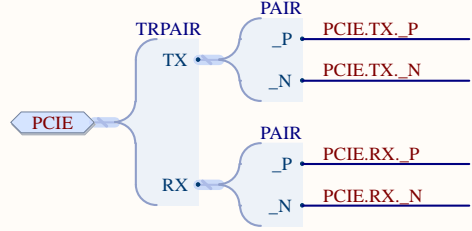
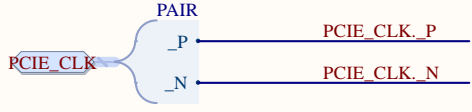
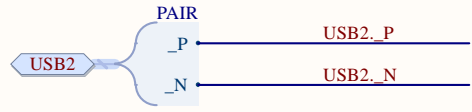
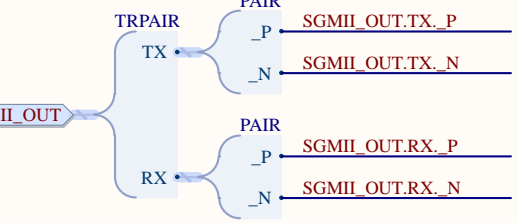
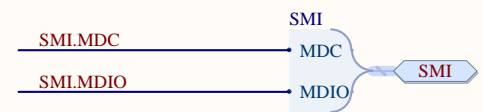
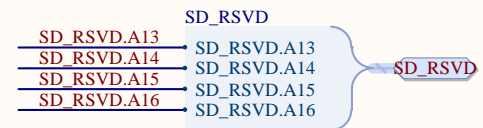
C

D

D



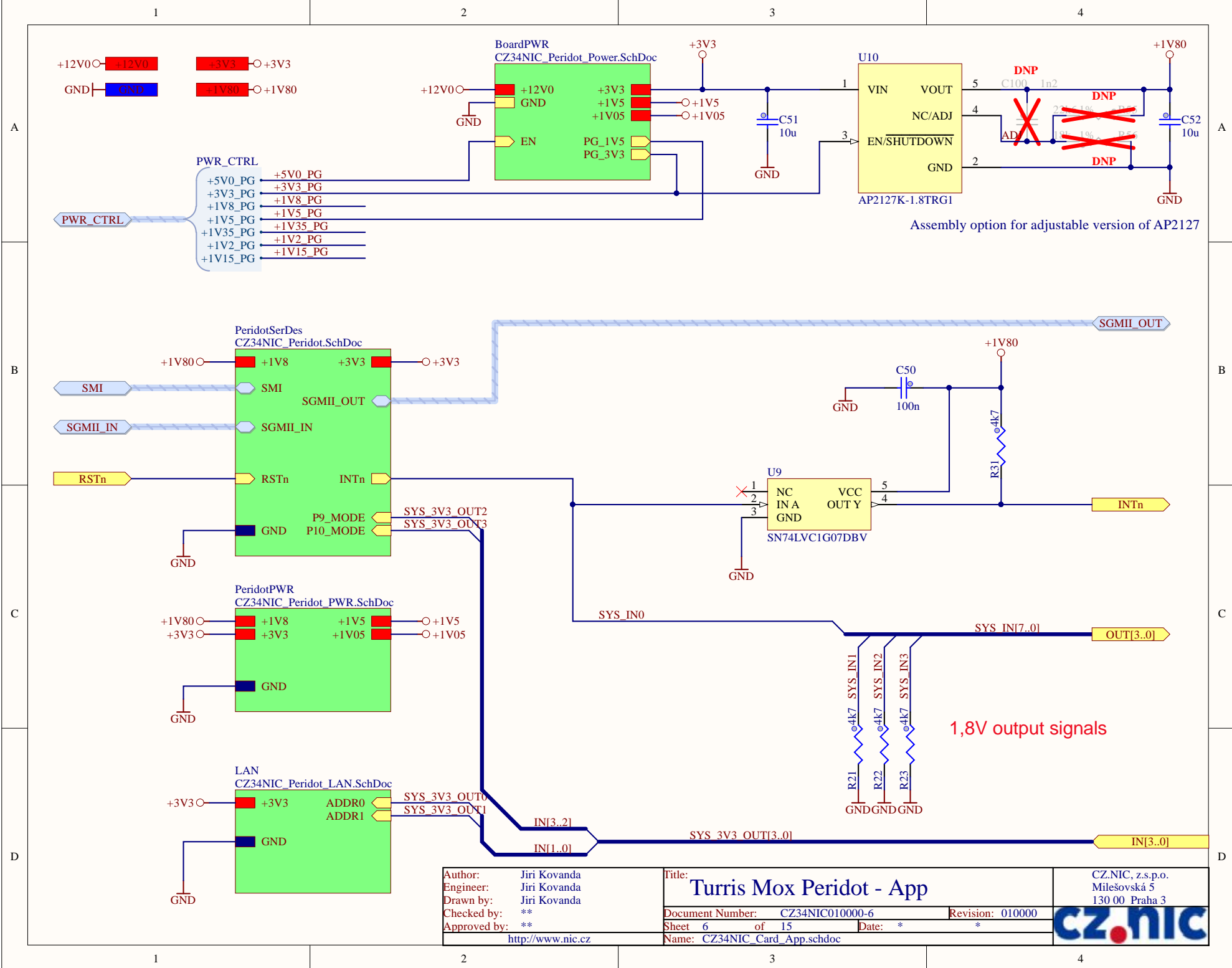
P2		P2	
B	A	B	A
GND	B1	A1	GND
+12V0	B2	A2	+12V0
+12V0	B3	A3	+12V0
+5V0_PG	B4	A4	MISO_DEV
+3V3_PG	B5	A5	MOSI_DEV
+1V8_PG	B6	A6	SCK
+1V5_PG	B7	A7	SSn
+1V35_PG	B8	A8	SYSRSTn
+1V2_PG	B9	A9	DEVRSTn
+1V15_PG	B10	A10	INTn
GND	B11	A11	
GND	B12	A12	GND
SD.RX_P	B13	A13	SD_RSVD.A13
SD.RX_N	B14	A14	SD_RSVD.A14
SD.TX_P	B15	A15	SD_RSVD.A15
SD.TX_N	B16	A16	SD_RSVD.A16
GND	B17	A17	GND
SGMII_OUT.TX_N	B18	A18	SMI.MDC
SGMII_OUT.TX_P	B19	A19	SMI.MDIO
SGMII_OUT.RX_N	B20	A20	
SGMII_OUT.RX_P	B21	A21	
GND	B22	A22	GND
USB2_P	B23	A23	I2C.SCL
USB2_N	B24	A24	I2C.SDA
PCIE.RX_N	B25	A25	
PCIE.RX_P	B26	A26	
GND	B27	A27	GND
PCIE.TX_N	B28	A28	PCIE_CTRL.RESETn
PCIE.TX_P	B29	A29	PCIE_CTRL.CLKREQ
PCIE_CLK_P	B30	A30	
PCIE_CLK_N	B31	A31	
GND	B32	A32	GND



Author: Jiri Kovanda
 Engineer: Jiri Kovanda
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Title: **Turris Mox Peridot - Out CN**
 Document Number: CZ34NIC010000-5
 Sheet 5 of 15
 Name: CZ34NIC_SYS_OUT_CN.SchDoc

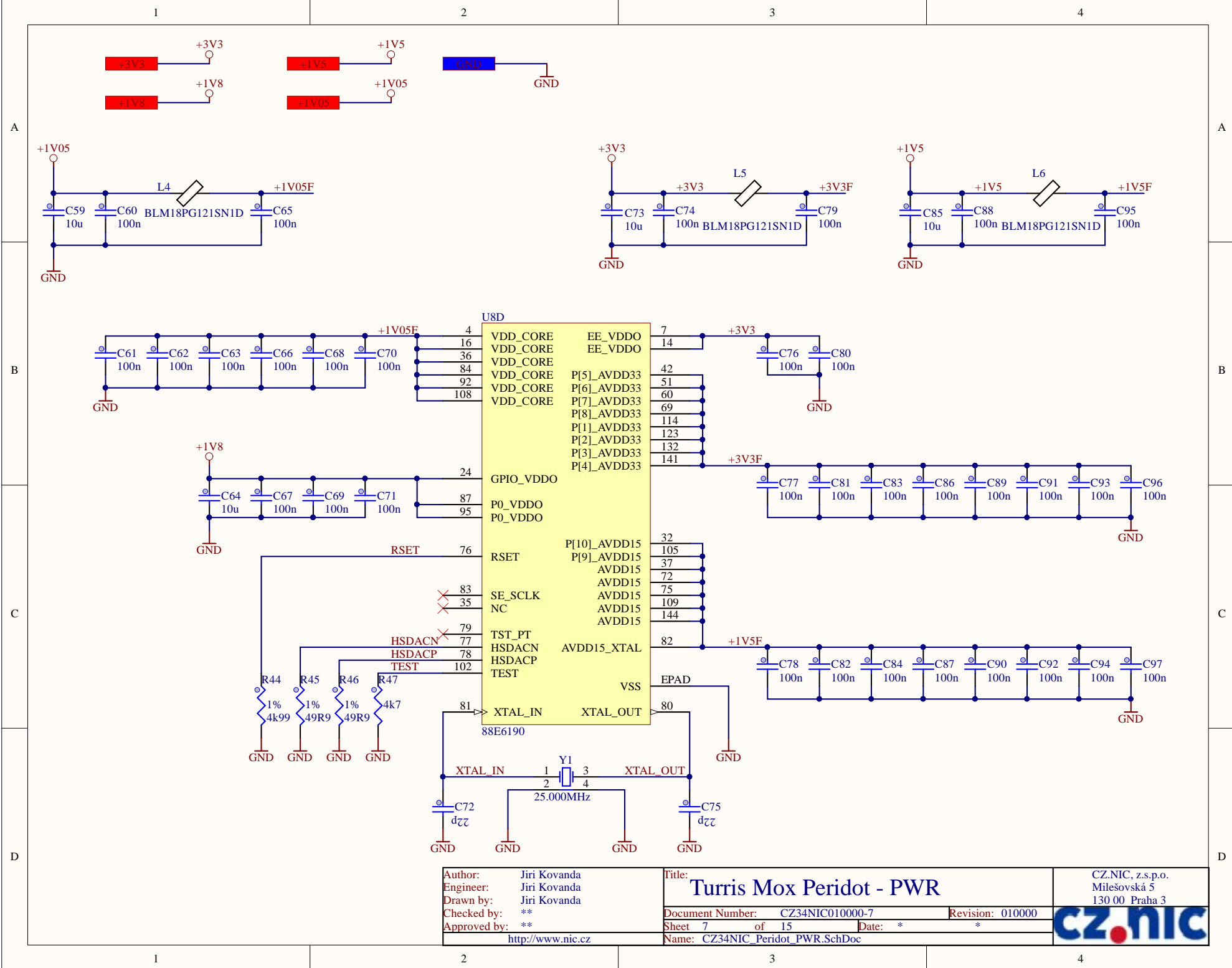
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Author: Jiri Kovanda
 Engineer: Jiri Kovanda
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 Checked by: **
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Title: **Turris Mox Peridot - App**
 Document Number: CZ34NIC010000-6
 Sheet 6 of 15
 Name: CZ34NIC_Card_App.schdoc
 Revision: 010000
 Date: * * *

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Title: **Turrus Mox Peridot - PWR**
 Document Number: CZ34NIC010000-7
 Sheet 7 of 15
 Name: CZ34NIC_Peridot_PWR.SchDoc
 Revision: 010000
 Date: * *

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A

A

B

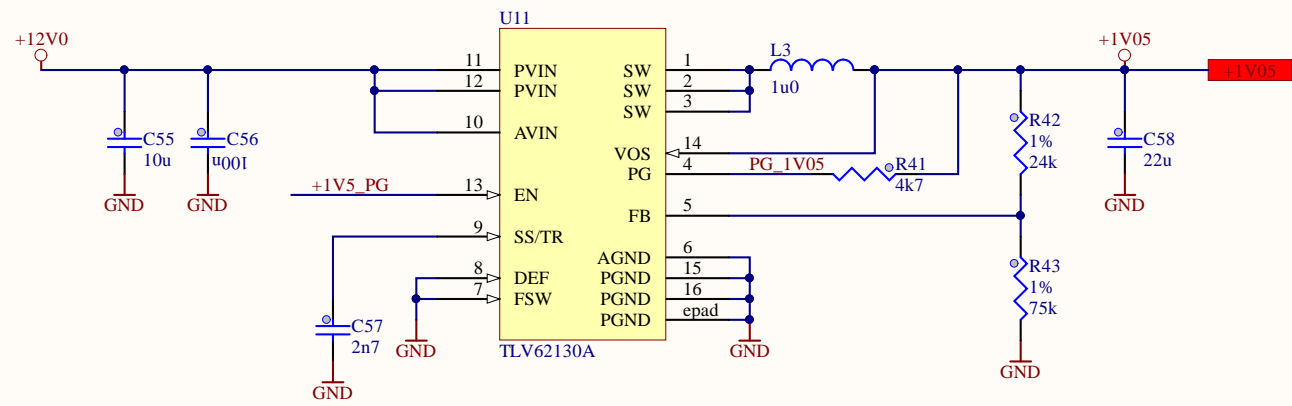
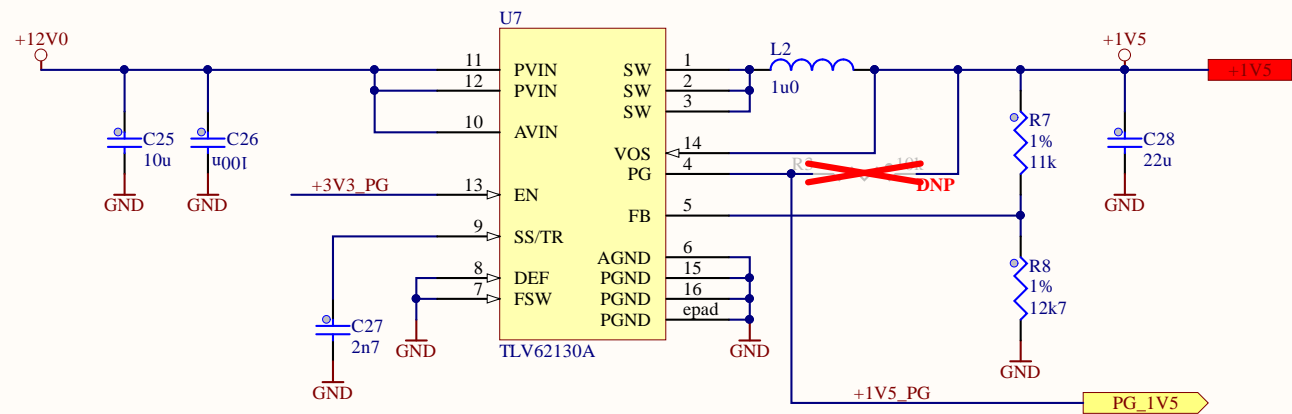
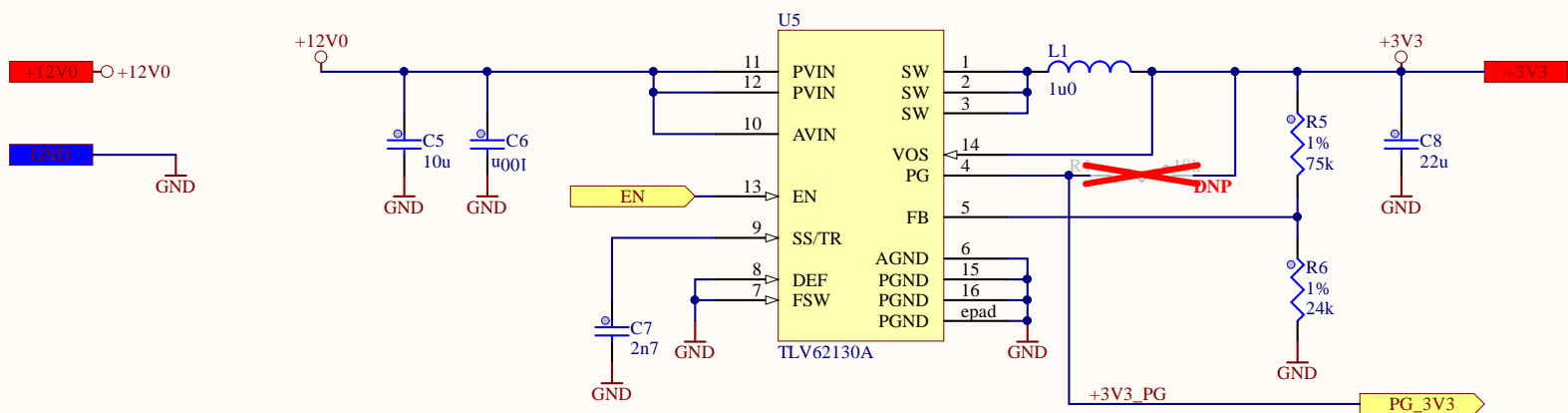
B

C

C

D

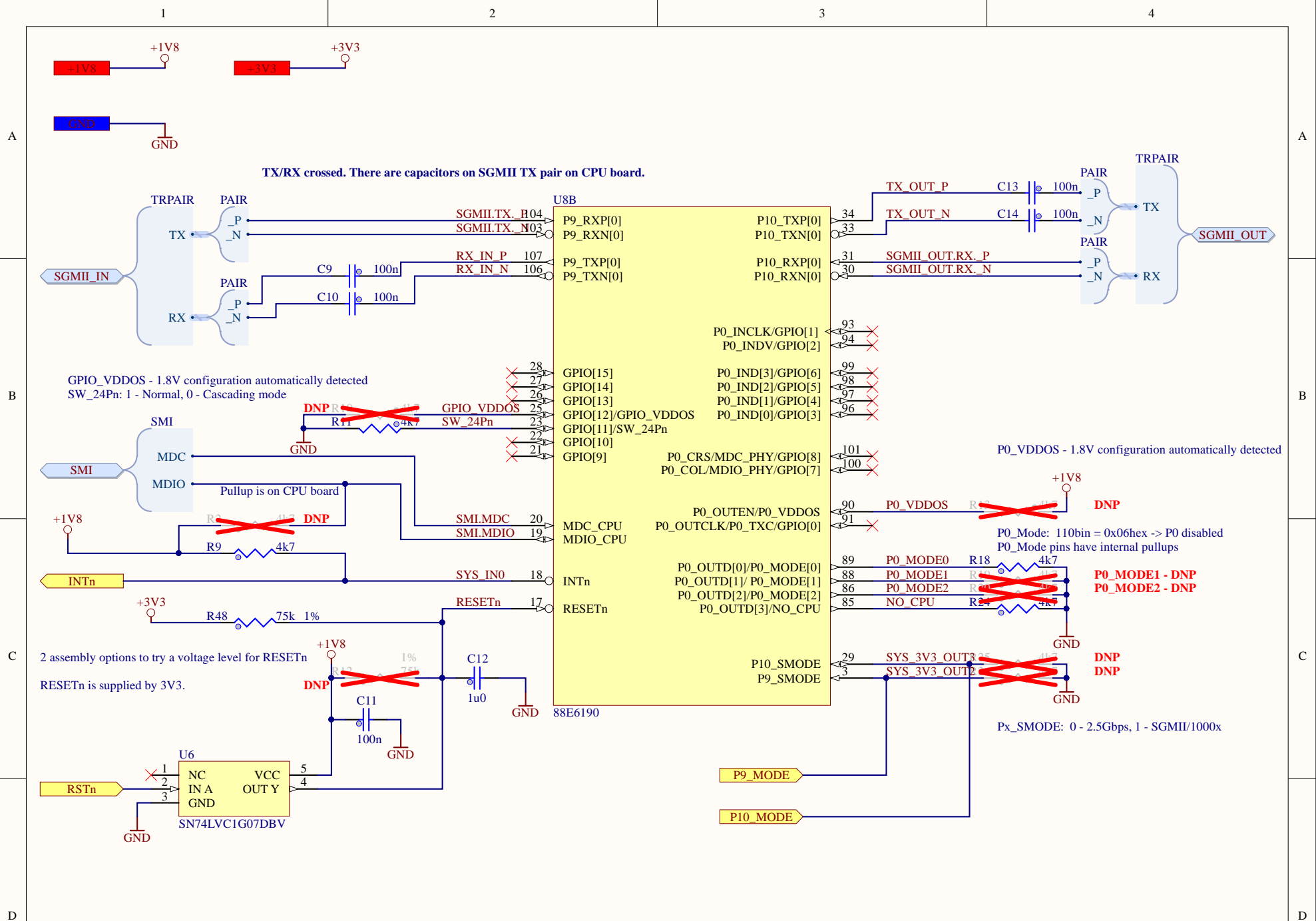
D



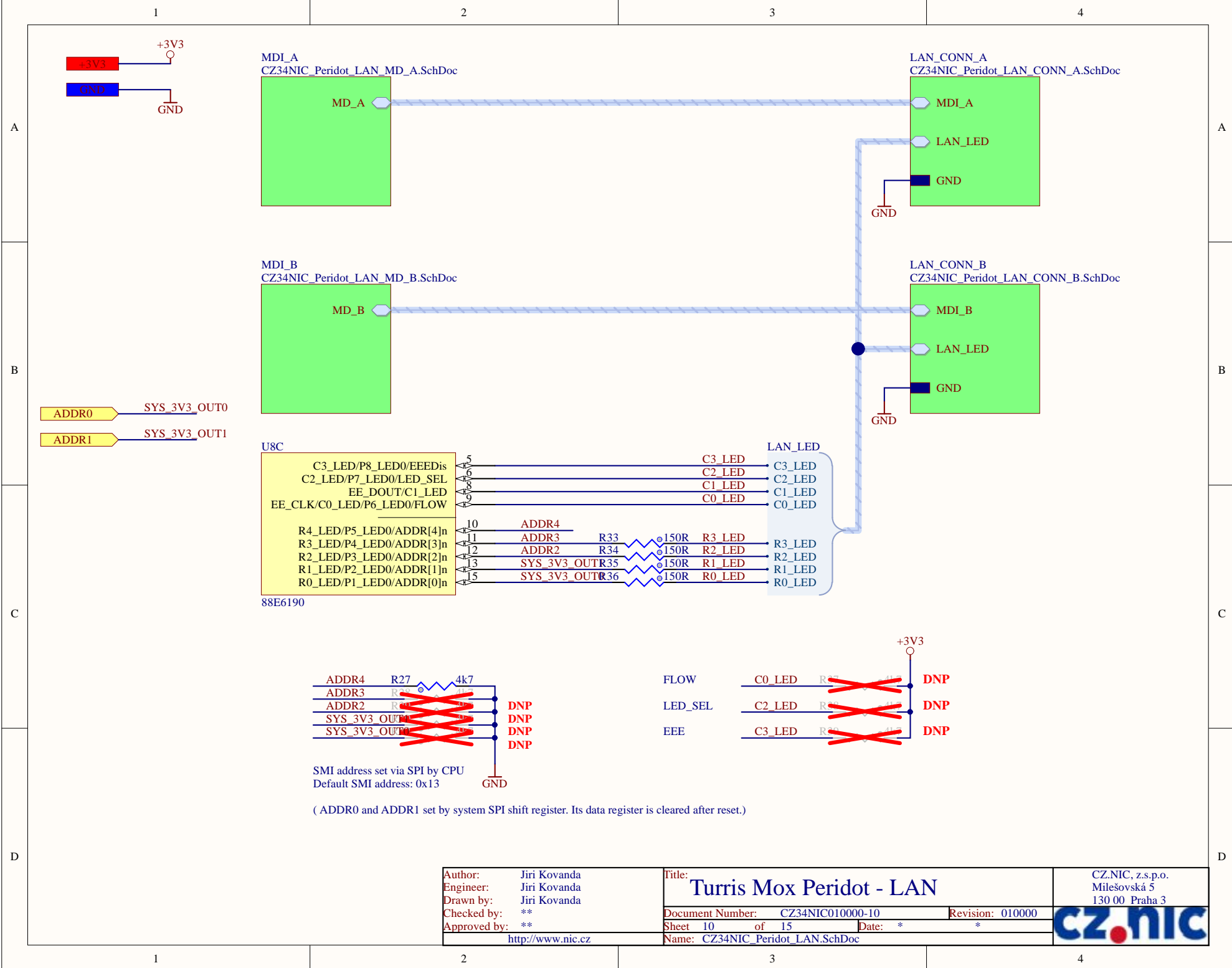
Author: Jiri Kovanda
 Engineer: Jiri Kovanda
 Drawn by: Jiri Kovanda
 Checked by: **
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Title: **Turris Mox Peridot - Power**
 Document Number: CZ34NIC010000-8
 Sheet 8 of 15
 Name: CZ34NIC_Peridot_Power.SchDoc

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Author:	Jiri Kovanda	Title:	Turris Mox Peridot - Serdes, SMI	CZ.NIC, z.s.p.o. Milešovská 5 130 00 Praha 3
Engineer:	Jiri Kovanda	Document Number:	CZ34NIC010000-9	Revision: 010000
Drawn by:	Jiri Kovanda	Sheet	9 of 15	Date: * *
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MDI_A
CZ34NIC_Peridot_LAN_MD_A.SchDoc

MD_A

LAN_CONN_A
CZ34NIC_Peridot_LAN_CONN_A.SchDoc

MDI_A
LAN_LED
GND

MDI_B
CZ34NIC_Peridot_LAN_MD_B.SchDoc

MD_B

LAN_CONN_B
CZ34NIC_Peridot_LAN_CONN_B.SchDoc

MDI_B
LAN_LED
GND

ADDR0 → SYS_3V3_OUT0
ADDR1 → SYS_3V3_OUT1

U8C

C3_LED/P8_LED0/EEEDis	5	C3_LED	5
C2_LED/P7_LED0/LED_SEL	6	C2_LED	6
EE_DOUT/C1_LED	7	C1_LED	7
EE_CLK/C0_LED/P6_LED0/FLOW	8	C0_LED	8
R4_LED/P5_LED0/ADDR[4]n	10	ADDR4	10
R3_LED/P4_LED0/ADDR[3]n	11	ADDR3	11
R2_LED/P3_LED0/ADDR[2]n	12	ADDR2	12
R1_LED/P2_LED0/ADDR[1]n	13	SYS_3V3_OUTR35	13
R0_LED/P1_LED0/ADDR[0]n	15	SYS_3V3_OUTR36	15

LAN_LED

C3_LED	R33	150R	R3_LED	3
C2_LED	R34	150R	R2_LED	4
C1_LED	R35	150R	R1_LED	5
C0_LED	R36	150R	R0_LED	6

88E6190

ADDR4	R27	4k7	DNP
ADDR3	R28	4k7	DNP
ADDR2	R29	4k7	DNP
SYS_3V3_OUT1	R30	4k7	DNP
SYS_3V3_OUT0	R31	4k7	DNP

SMI address set via SPI by CPU
Default SMI address: 0x13

FLOW	C0_LED	R32	4k7	DNP
LED_SEL	C2_LED	R33	4k7	DNP
EEE	C3_LED	R34	4k7	DNP

(ADDR0 and ADDR1 set by system SPI shift register. Its data register is cleared after reset.)

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Engineer: Jiri Kovanda	Document Number: CZ34NIC010000-10	Revision: 010000
Drawn by: Jiri Kovanda	Sheet 10 of 15	Date: * *
Checked by: **	Name: CZ34NIC_Peridot_LAN.SchDoc	
Approved by: **		
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A

A

B

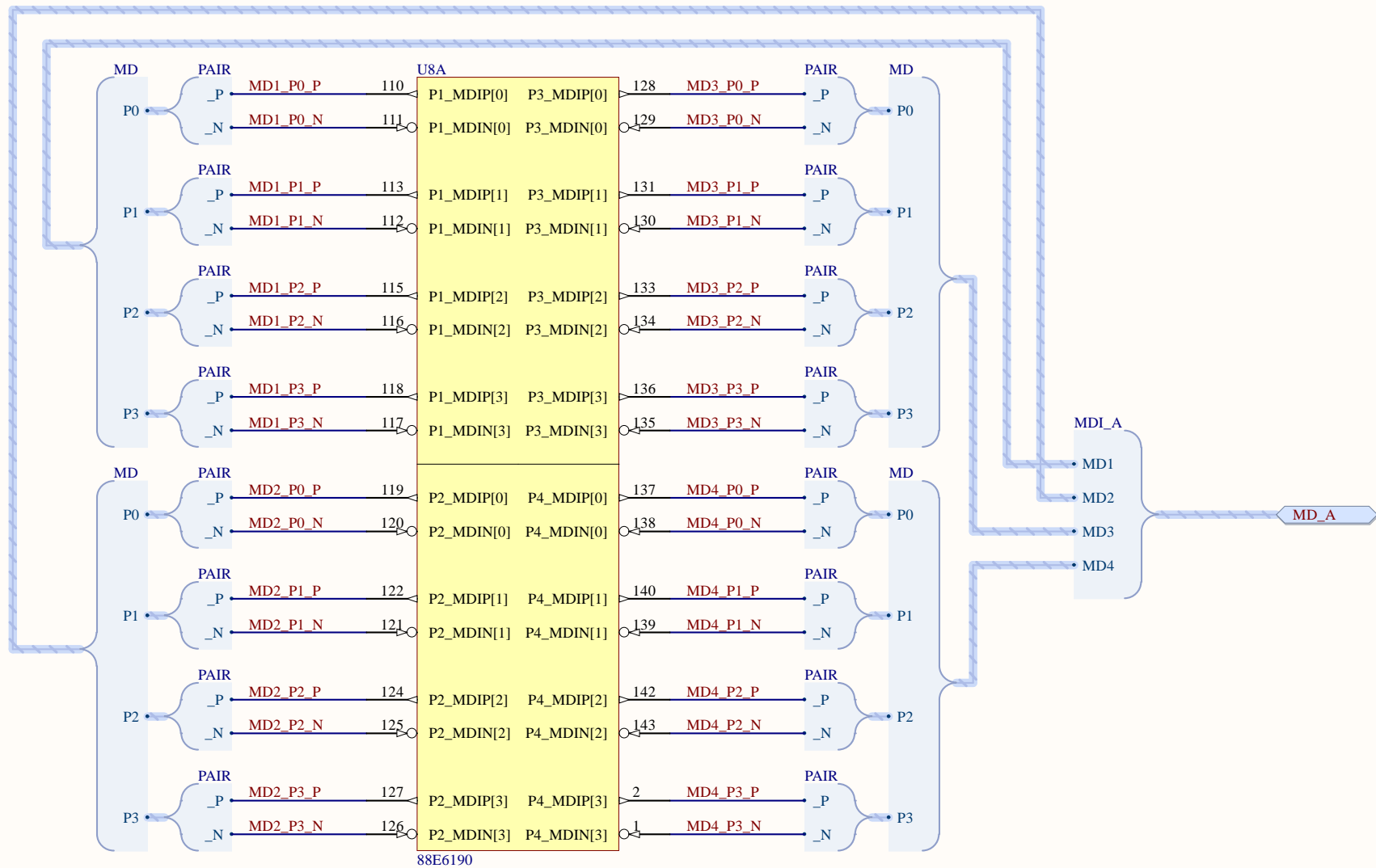
B

C

C

D

D



88E6190

Author: Jiri Kovanda
 Engineer: Jiri Kovanda
 Drawn by: Jiri Kovanda
 Checked by: **
 Approved by: **
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Title: **Turris Mox Peridot - LAN**
 Document Number: CZ34NIC010000-11 Revision: 010000
 Sheet 11 of 15 Date: * *
 Name: CZ34NIC_Peridot_LAN_MD_A.SchDoc

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A

A

B

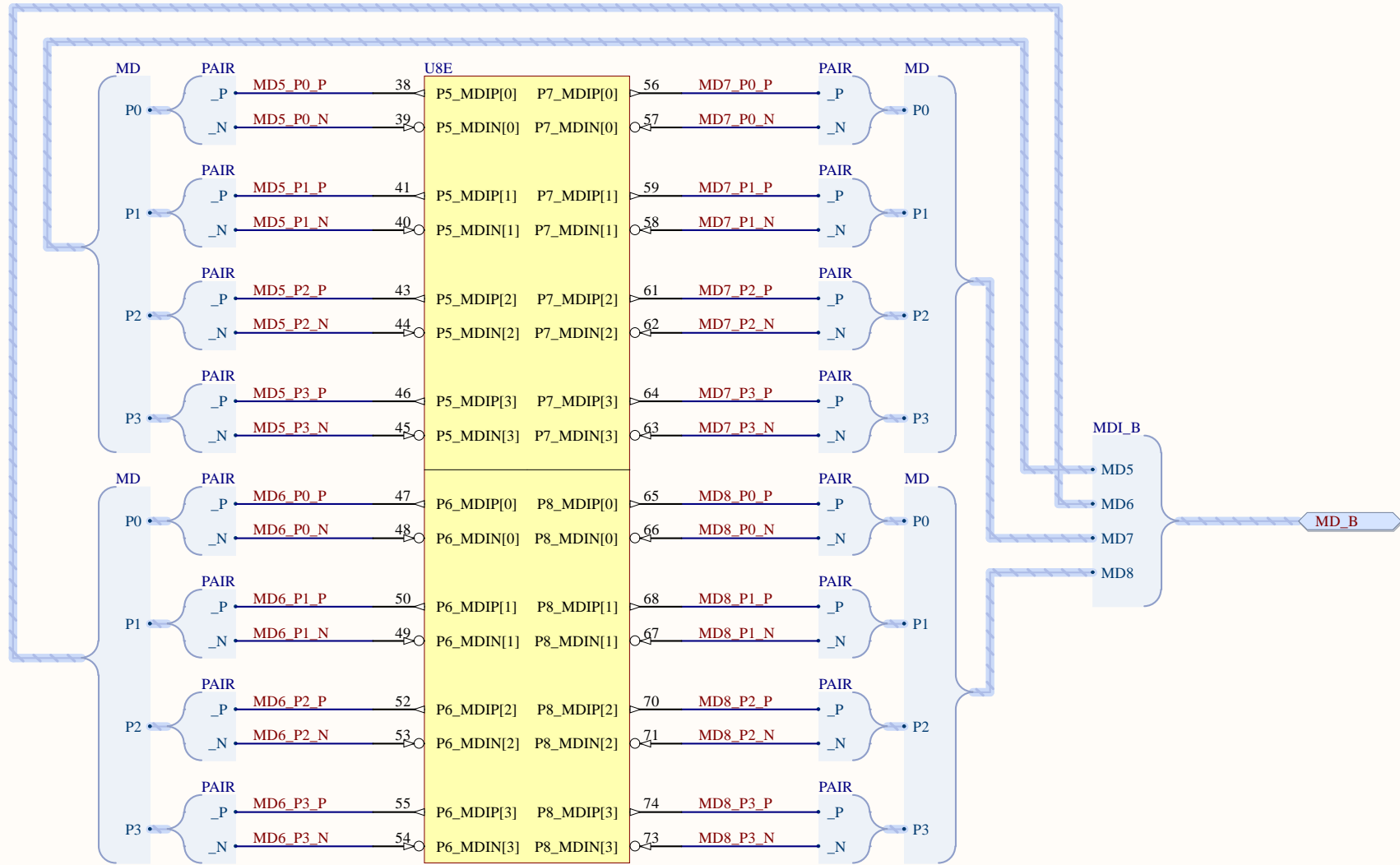
B

C

C

D

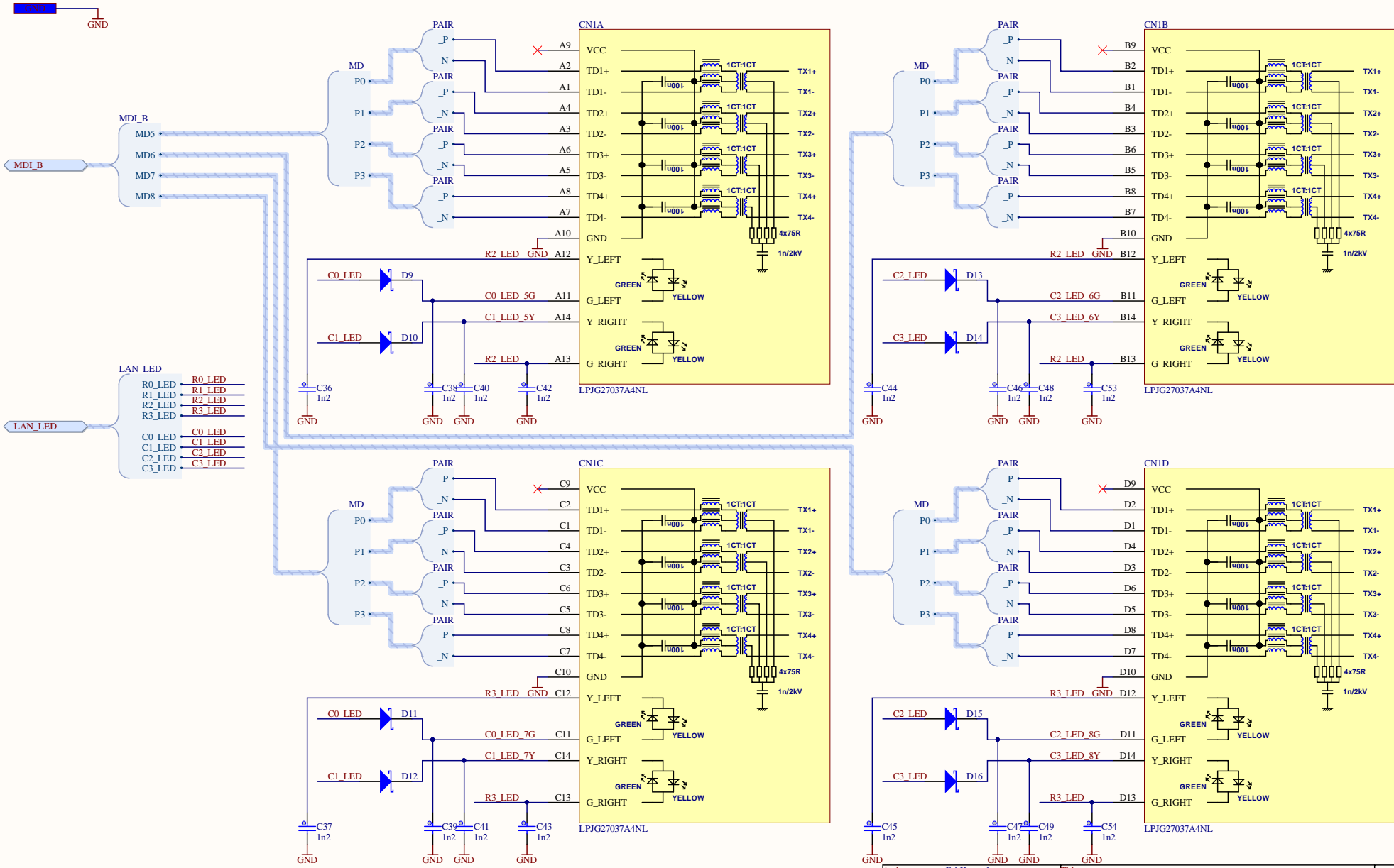
D



Author: Jiri Kovanda
 Engineer: Jiri Kovanda
 Drawn by: Jiri Kovanda
 Checked by: **
 Approved by: **
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Title: **Turris Mox Peridot - LAN**
 Document Number: CZ34NIC010000-12
 Sheet 12 of 15
 Name: CZ34NIC_Peridot_LAN_MD_B.SchDoc

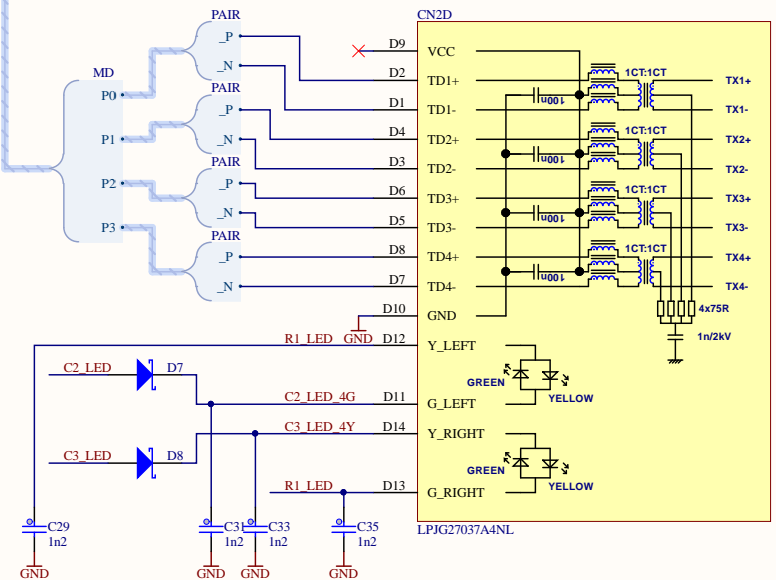
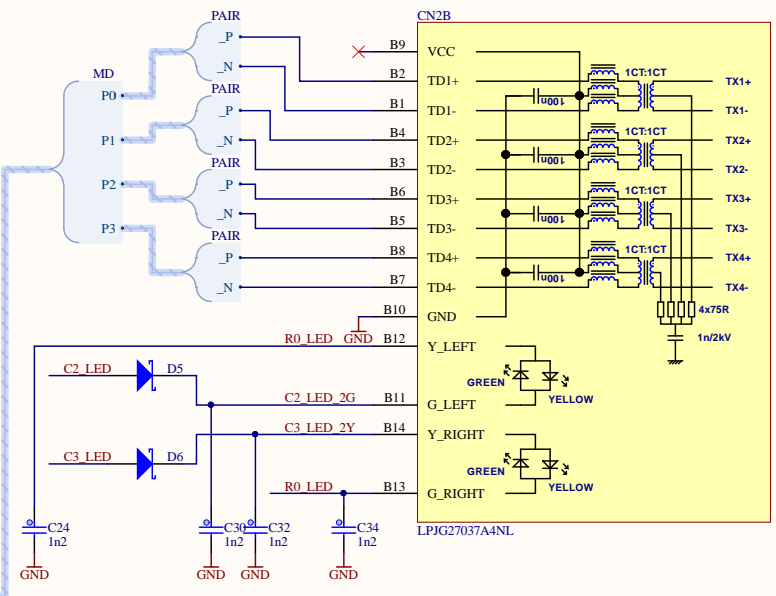
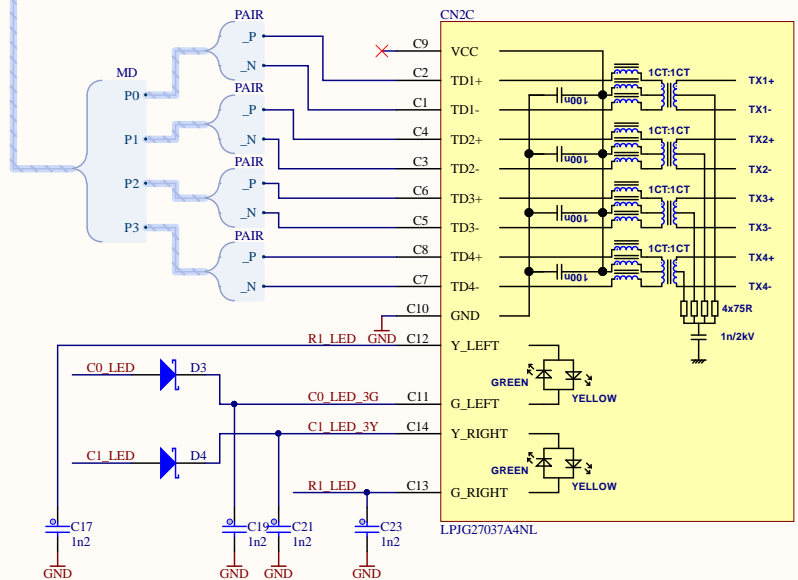
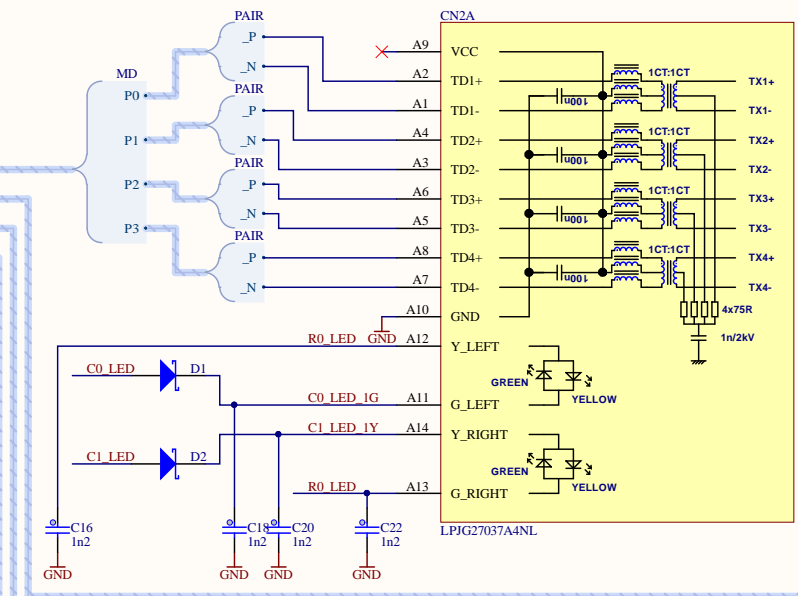
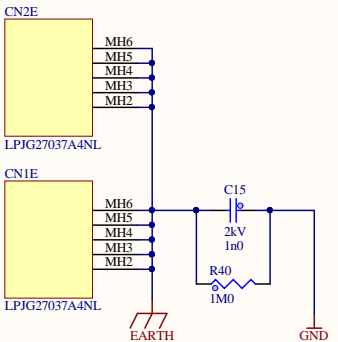
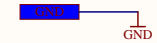
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Author: Jiri Kovanda
 Engineer: Jiri Kovanda
 Drawn by: Jiri Kovanda
 Checked by: **
 Approved by: **
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Title: **Turris Mox Peridot - LAN connector**
 Document Number: CZ34NIC010000-13
 Sheet 13 of 15
 Date: *
 Revision: 010000

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Title: **Turris Mox Peridot - LAN connector**
 Document Number: CZ34NIC010000-L4
 Sheet 14 of 15
 Date: *
 Revision: 010000

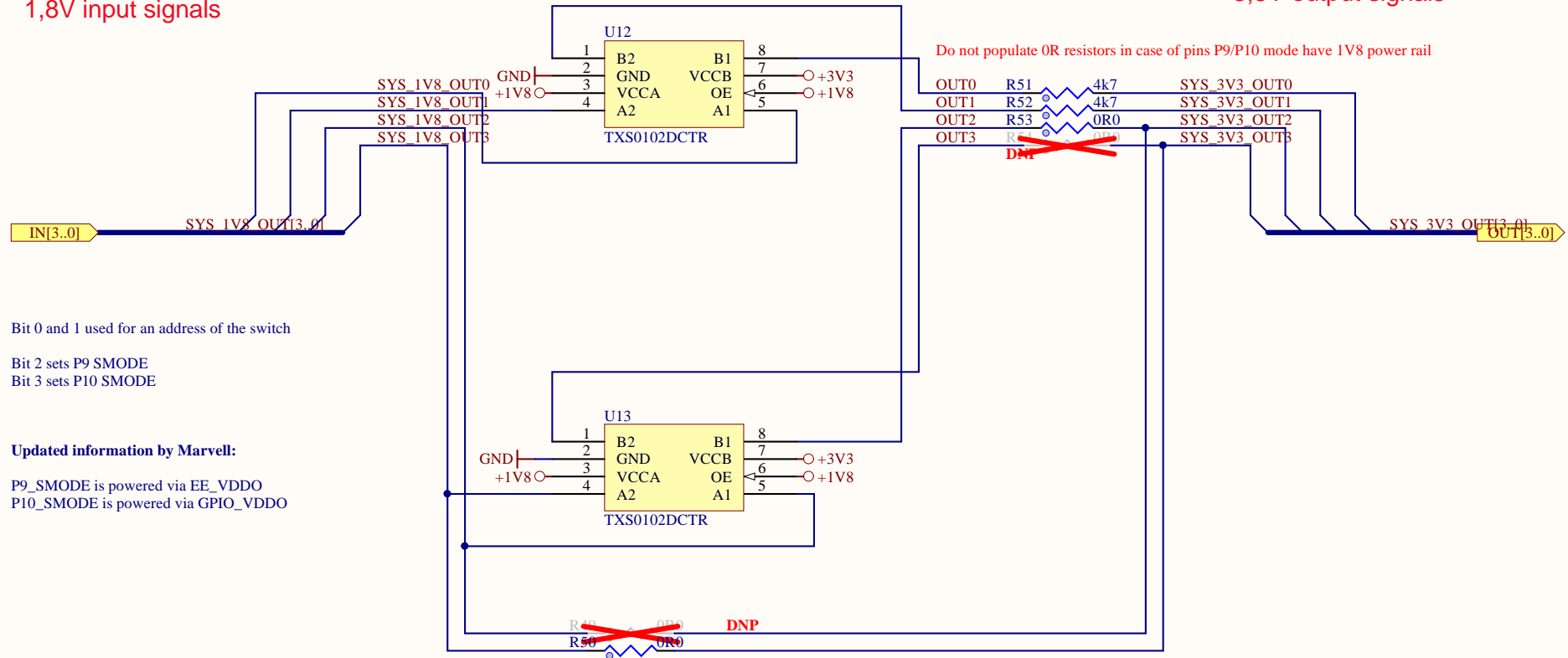


+3V3  +3V3
 GND  GND +1V8  +1V8



1,8V input signals

3,3V output signals



Bit 0 and 1 used for an address of the switch
 Bit 2 sets P9 SMODE
 Bit 3 sets P10 SMODE

Updated information by Marvell:

P9_SMODE is powered via EE_VDDO
 P10_SMODE is powered via GPIO_VDDO

Populate OR resistors in case of pins P9/P10 mode have 1V8 power rail

Author: Jiri Kovanda
 Engineer: Jiri Kovanda
 Drawn by: Jiri Kovanda
 Checked by: **
 Approved by: **
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Title: **Turris Mox Peridot - Level Shifter**

Document Number: CZ34NIC010000-15 Revision: 010000
 Sheet 15 of 15 Date: * *
 Name: CZ34NIC_LEVEL_SH.schdoc

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